# Lecture No 8

## Introduction

- Time
- cost-area
- technology state of the art
- the economics of a processor project: A study
- instruction sets
- professor evaluation matrix

# Time, area and instruction sets

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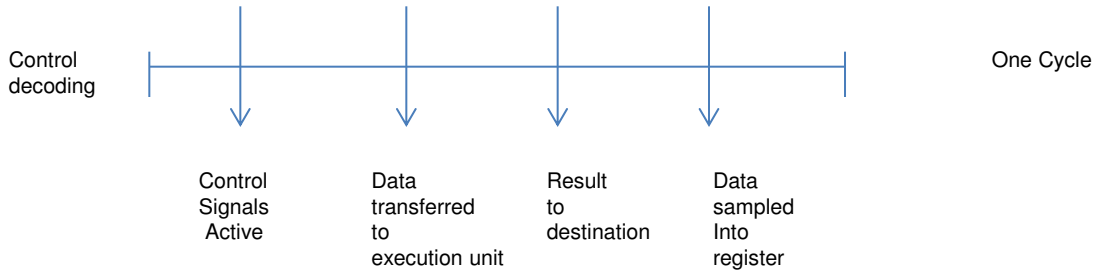
# *Time*

- Time include partitioning instruction into cycle.
- In a pipelined processors, data flows through stages
- Within limits, the shorter time is more productive.

# The Nature of Cycle

- A Cycle is defined as  the time between state transition.
- The designer determines the cycle by finding worst case time .
- The time must be sufficient for data to be sampled into designated destination register.




Possible sequence of actions within a cycle

# Partitioning Instruction Execution into Cycles

Instruction Execution has following cycles in sequential order

- Instruction Fetch
- Decode
- Register Fetch
- Address Generate
- Translate
- Data Fetch
- Execute
- Put Away